GATED DIODE MEMORY CELLS

ABSTRACT

A gated diode memory cell is provided, including one or more transistors, such as field effect transistors ("FETs"), and a gated diode in signal communication with the FETs such that the gate of the gated diode is in signal communication with the source of a first FET, wherein the gate of the gated diode forms one terminal of the storage cell and the source of the gated diode forms another terminal of the storage cell, the drain of the first FET being in signal communication with a bitline ("BL") and the gate of the first FET being in signal communication with a write wordline ("WLw"), and the source of the gated diode being in signal communication with a read wordline ("WLr").